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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2188	16

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,017	SAULSBURY ET AL.	
	Examiner	Art Unit	
	Gary J Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13, 14*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 and 5 were amended by Applicant. Claims 1-19 are pending.

2. It is noted that while the previous Office action mailed September 5, 2003, was labeled on each of it's pages Paper No. 14, it was subsequently labeled on the cover sheet and in the file as Paper No. 12, and will be considered Paper No. 12 henceforth.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on November 6 and 13, 2003 (paper nos. 13 and 14) were considered by the examiner.

Claim Objections

4. Claims are objected to because of the following informalities: Claim 4 at lines 2-3, "said at least one bank of memory on said other processor chips" lacks proper antecedent basis. Claim 5 at lines 9-10, "said at least one bank or memory on said other processor chips" lacks proper antecedent basis. Claim 8 at line 3, "one or more processor chips" is objected to since at lines 10-11 it wouldn't make sense to communicate with other processors if there were only one. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz et al., U.S. Patent 6,321,318 B1, in view of Kozyrakis et al., "Scalable Processors in the Billion-Transistor Era: IRAM".

7. As to claim 1, Baltz discloses a processor chip (Fig. 1) including core 20, at least one bank of memory 31 with mode control input (controlled by PCC field, see col. 7 line 57 to col. 8 line 17) controlling the memory mode between physical memory and cache memory, on a single chip (see col. 1 line 66 to col. 2 line 37). Baltz does not disclose that the memory is DRAM. However, Kozyrakis describes the advantages of integrating DRAM memory, rather than SRAM, for the purpose of increasing overall performance by reducing external bus bandwidth requirements, improving on-chip memory capacity, and also reducing power consumption (see page 75, entire second column and including the entire last paragraph concluded on page 76). An artisan would have recognized that the advantages of both of these references would readily combine; that is, one could achieve the benefits of a DRAM having higher on-chip capacity with lower external bandwidth requirement and lower power consumption while also having the benefit of a reconfigurable cache or physical memory on-chip memory. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use DRAM in the system of Baltz, or alternatively to provide reconfigurability between cache and physical memory modes for the DRAM of Kozyrakis, because the advantages of flexibility for different applications are achieved by the reconfigurability and the advantages of improved performance without increased bandwidth requirement and power consumption are achieved by the DRAM.

8. Claims 2-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al., U.S. Patent 5,710,907, in view of Hsu et al., U.S. Patent 6,128,700, and further in view of Kozyrakis et al., "Scalable Processors in the Billion-Transistor Era: IRAM".

9. As to claims 2 and 8, Hagersten discloses a processing core (311x, Fig. 3A), at least one bank of memory (313x) including mode controlling input (for example, whether local address space or global, or result of COMA counters to control mode) controlling mode of the memory between a physical memory mode (NUMA, in which each memory has it's own part of the address space, Fig. 1B) and a cache mode (COMA, in which each memory caches addresses that have been attracted to it's COMA cache 314, see also Figs. 2B and 2C). See also Abstract, Figs. 3C, 3E, and 3F, col. 6 lines 25-52, col. 7 lines 1-33. The memory bank is in the mode as recited for each individual access. Hagersten also discloses as recited I/O link (interconnect 390, Fig. 3A) and communication and memory controller (interface 315 and MMU 312x), which control, receive, and process requests as recited.

Hagersten does not disclose that the memory is DRAM. However, Hsu describes using DRAM for an analogous second level cache (see Abstract), because DRAM cells use less space (thus increasing density) and is less expensive than SRAM (see col. 2 lines 43-58, and col. 3 lines 19-29). The advantages of reducing the space needed while also reducing the cost would have motivated an artisan to implement the second level caches of Hagersten with DRAM. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use DRAM, because it was

known to reduce the space needed (or increase the density) and reduce the cost of second level caches.

Neither Hagersten nor Hsu disclose that the processors and associated memory are on the same chip. However, Kozyrakis describes the advantages of integrating DRAM memory, rather than SRAM, for the purpose of increasing overall performance by reducing external bus bandwidth requirements, improving on-chip memory capacity, and also reducing power consumption (see page 75, entire second column and including the entire last paragraph concluded on page 76). An artisan would have recognized that these advantages would be applicable to the system of Hagersten when incorporating a DRAM as taught by Hsu; that is, one could achieve the benefits of a DRAM having higher on-chip capacity with lower external bandwidth requirement and lower power consumption. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use integrate the processor and DRAM in the system of Hagersten, because the advantages of improved performance without increased bandwidth requirement and power consumption are achieved by integrating the processors and associated DRAM.

10. As to claims 3 and 9, 312x and 315 as stated with regard to claim 2 may be seen as the recited first and second controllers respectively.

11. As to claims 4 and 10, in NUMA as stated with regard to claim 1, the addresses and therefore the data is different on different banks.

12. As to claims 5-7 and 11-13, an external memory interface may be seen as the interface to any of the other memories 323x, 383x.

13. As to claim 14, first and second processor chips is disclosed in Hagersten as cited above.

14. As to claim 15, Hagersten discloses the recited request from first to second processor memory (as cited hereinabove, and further at col. 6 lines 30-43).

15. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al., U.S. Patent 5,710,907, in view of Kozyrakis et al., "Scalable Processors in the Billion-Transistor Era: IRAM".

16. As to claim 16, Hagersten discloses the recited method a first processor 311x of accessing memory on a second (another 311x, or 321x or 381x), comprising issuing a request, determining if the data is on the first processor's memory or the second (at 313x, or 323x or 383x), communicating the request to the second if there, accessing the memory of the second processor, and communicating the result to the first processor. See Abstract, Figs. 3A-3F, col. 6 line 5-52, col. 7 lines 1-33.

Hagersten does not disclose that the processors and associated memory are on the same chip. However, Kozyrakis describes the advantages of integrating (DRAM) memory, for the purpose of increasing overall performance by reducing external bus bandwidth requirements, improving on-chip memory capacity, and also reducing power consumption (see page 75, entire second column and including the entire last paragraph concluded on page 76). Clearly these advantages are achieved in part from the integration on-chip, and not just via the use of DRAM. An artisan would have recognized that these advantages would be applicable to the system of Hagersten, and that one could achieve the benefits of an on-chip memory with lower external bandwidth

requirement and lower power consumption. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use integrate the processor and memory in the system of Hagersten, because the advantages of improved performance without increased bandwidth requirement and power consumption are achieved by integrating the processors and associated memory.

17. As to claim 17, the memories each are physical memory (for example, when in NUMA mode).

18. As to claim 18, the memories are each caches (for example, when in COMA mode).

19. As to claim 19, the memories comprise mode control inputs that switch from physical memory to cache mode (for example, whether local address space or global, or result of COMA counters to control mode).

Conclusion

20. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on November 6 and 17, 2003, prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J Portka whose telephone number is (703) 305-4033. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J Portka
Primary Examiner
Art Unit 2188

May 11, 2004